

# *Contents*

<b>Preface</b>	<i>ix</i>
<b>1 Fundamentals</b>	<b>1</b>
1.1 Frequency and Time	<i>1</i>
1.2 Time and Distance	<i>6</i>
1.3 Lumped Versus Distributed Systems	<i>7</i>
1.4 A Note About 3 dB and RMS Frequencies	<i>8</i>
1.5 Four Kinds of Reactance	<i>10</i>
1.6 Ordinary Capacitance	<i>11</i>
1.7 Ordinary Inductance	<i>17</i>
1.8 A Better Method for Estimating Decay Time	<i>22</i>
1.9 Mutual Capacitance	<i>25</i>
1.10 Mutual Inductance	<i>29</i>
<b>2 High-Speed Properties of Logic Gates</b>	<b>37</b>
2.1 Historical Development of a Very Old Digital Technology	<i>37</i>
2.2 Power	<i>39</i>
2.3 Speed	<i>59</i>
2.4 Packaging	<i>66</i>

<b>3</b>	<b>Measurement Techniques</b>	<b>83</b>	
3.1	Rise Time and Bandwidth of Oscilloscope Probes	83	
3.2	Self-inductance of a Probe Ground Loop	86	
3.3	Spurious Signal Pickup from Probe Ground Loops	92	
3.4	How Probes Load Down a Circuit	95	
3.5	Special Probing Fixtures	98	
3.6	Avoiding Pickup from Probe Shield Currents	104	
3.7	Viewing a Serial Data Transmission System	108	
3.8	Slowing Down the System Clock	110	
3.9	Observing Crosstalk	111	
3.10	Measuring Operating Margins	113	
3.11	Observing Metastable States	120	
<b>4</b>	<b>Transmission Lines</b>	<b>133</b>	
4.1	Shortcomings of Ordinary Point-to-Point Wiring	133	
4.2	Infinite Uniform Transmission Line	140	
4.3	Effects of Source and Load Impedance	160	
4.4	Special Transmission Line Cases	167	
4.5	Line Impedance and Propagation Delay	178	
<b>5</b>	<b>Ground Planes and Layer Stacking</b>	<b>189</b>	
5.1	High-Speed Current Follows the Path of Least Inductance	189	
5.2	Crosstalk in Solid Ground Planes	191	
5.3	Crosstalk in Slotted Ground Planes	194	
5.4	Crosstalk in Cross-Hatched Ground Planes	197	
5.5	Crosstalk with Power and Ground Fingers	199	
5.6	Guard Traces	201	
5.7	Near-End and Far-End Crosstalk	204	
5.8	How to Stack Printed Circuit Board Layers	212	
<b>6</b>	<b>Terminations</b>	<b>223</b>	
6.1	End Terminators	223	
6.2	Source Terminators	231	
6.3	Middle Terminators	235	
6.4	AC Biasing for End Terminators	236	
6.5	Resistor Selection	239	
6.6	Crosstalk in Terminators	244	
<b>7</b>	<b>Vias</b>	<b>249</b>	
7.1	Mechanical Properties of Vias	249	
7.2	Capacitance of Vias	257	
7.3	Inductance of Vias	258	
7.4	Return Current and Its Relation to Vias	260	

<b>8</b>	<b>Power Systems</b>	<b>263</b>
8.1	Providing a Stable Voltage Reference	263
8.2	Distributing Uniform Voltage	268
8.3	Everyday Distribution Problems	279
8.4	Choosing a Bypass Capacitor	281
<b>9</b>	<b>Connectors</b>	<b>295</b>
9.1	Mutual Inductance—How Connectors Create Crosstalk	295
9.2	Series Inductance—How Connectors Create EMI	300
9.3	Parasitic Capacitance—Using Connectors on a Multidrop Bus	305
9.4	Measuring Coupling in a Connector	309
9.5	Continuity of Ground Underneath a Connector	312
9.6	Fixing EMI Problems with External Connections	314
9.7	Special Connectors for High-Speed Applications	316
9.8	Differential Signaling Through a Connector	319
9.9	Power Handling Features of Connectors	321
<b>10</b>	<b>Ribbon Cables</b>	<b>323</b>
10.1	Ribbon Cable Signal Propagation	324
10.2	Ribbon Cable Crosstalk	329
10.3	Ribbon Cable Connectors	336
10.4	Ribbon Cable EMI	338
<b>11</b>	<b>Clock Distribution</b>	<b>341</b>
11.1	Timing Margin	341
11.2	Clock Skew	343
11.3	Using Low-Impedance Drivers	346
11.4	Using Low-Impedance Clock Distribution Lines	348
11.5	Source Termination of Multiple Clock Lines	350
11.6	Controlling Crosstalk on Clock Lines	352
11.7	Delay Adjustments	353
11.8	Differential Distribution	360
11.9	Clock Signal Duty Cycle	361
11.10	Canceling Parasitic Capacitance of a Clock Repeater	362
11.11	Decoupling Clock Receivers from the Clock Bus	364
<b>12</b>	<b>Clock Oscillators</b>	<b>367</b>
12.1	Using Canned Clock Oscillators	367
12.2	Clock Jitter	376

<b>Collected References</b>	<b>385</b>
<b>A Points to Remember</b>	<b>389</b>
<b>B Calculation of Rise Time</b>	<b>399</b>
<b>C MathCad Formulas</b>	<b>409</b>
<b>Index</b>	<b>441</b>