



CONTENTS

CHAPTER 1 **Introductory Concepts**

2

- 1-1 Introduction to Digital 1s and 0s 4
- 1-2 Numerical Representations 6
- 1-3 Digital and Analog Systems 9
- 1-4 Digital Number Systems 14
- 1-5 Representing Binary Quantities 18
- 1-6 Digital Circuits/Logic Circuits 20
- 1-7 Parallel and Serial Transmission 22
- 1-8 Memory 23
- 1-9 Digital Computers 24

CHAPTER 2 **Number Systems and Codes**

32

- 2-1 Binary-to-Decimal Conversions 34
- 2-2 Decimal-to-Binary Conversions 35
- 2-3 Hexadecimal Number System 37
- 2-4 BCD Code 42
- 2-5 The Gray Code 44
- 2-6 Putting It All Together 46
- 2-7 The Byte, Nibble, and Word 46
- 2-8 Alphanumeric Codes 48
- 2-9 Parity Method for Error Detection 50
- 2-10 Applications 53

CHAPTER 3 Describing Logic Circuits 64

- 3-1 Boolean Constants and Variables 67
- 3-2 Truth Tables 67
- 3-3 OR Operation with OR Gates 68
- 3-4 AND Operation with AND Gates 72
- 3-5 NOT Operation 75
- 3-6 Describing Logic Circuits Algebraically 76
- 3-7 Evaluating Logic-Circuit Outputs 78
- 3-8 Implementing Circuits from Boolean Expressions 81
- 3-9 NOR Gates and NAND Gates 83
- 3-10 Boolean Theorems 86
- 3-11 DeMorgan's Theorems 90
- 3-12 Universality of NAND Gates and NOR Gates 93
- 3-13 Alternate Logic-Gate Representations 96
- 3-14 Which Gate Representation to Use 99
- 3-15 Propagation Delay 105
- 3-16 Summary of Methods to Describe Logic Circuits 106
- 3-17 Description Languages Versus Programming Languages 108
- 3-18 Implementing Logic Circuits with PLDs 110
- 3-19 HDL Format and Syntax 112
- 3-20 Intermediate Signals 115

CHAPTER 4 Combinational Logic Circuits 128

- 4-1 Sum-of-Products Form 130
- 4-2 Simplifying Logic Circuits 131
- 4-3 Algebraic Simplification 132
- 4-4 Designing Combinational Logic Circuits 137
- 4-5 Karnaugh Map Method 143
- 4-6 Exclusive-OR and Exclusive-NOR Circuits 154
- 4-7 Parity Generator and Checker 159
- 4-8 Enable/Disable Circuits 161
- 4-9 Basic Characteristics of Digital ICs 163
- 4-10 Troubleshooting Digital Systems 170
- 4-11 Internal Digital IC Faults 172
- 4-12 External Faults 176
- 4-13 Troubleshooting Case Study 178
- 4-14 Programmable Logic Devices 180
- 4-15 Representing Data in HDL 187
- 4-16 Truth Tables Using HDL 191
- 4-17 Decision Control Structures in HDL 194

CHAPTER 5 Flip-Flops and Related Devices 218

- 5-1 NAND Gate Latch 221
- 5-2 NOR Gate Latch 226
- 5-3 Troubleshooting Case Study 229
- 5-4 Digital Pulses 230
- 5-5 Clock Signals and Clocked Flip-Flops 231
- 5-6 Clocked S-R Flip-Flop 234
- 5-7 Clocked J-K Flip-Flop 237
- 5-8 Clocked D Flip-Flop 240
- 5-9 D Latch (Transparent Latch) 242
- 5-10 Asynchronous Inputs 243
- 5-11 Flip-Flop Timing Considerations 246
- 5-12 Potential Timing Problem in FF Circuits 249
- 5-13 Flip-Flop Applications 251
- 5-14 Flip-Flop Synchronization 251
- 5-15 Detecting an Input Sequence 252
- 5-16 Data Storage and Transfer 253
- 5-17 Serial Data Transfer: Shift Registers 255
- 5-18 Frequency Division and Counting 258
- 5-19 Microcomputer Application 262
- 5-20 Schmitt-Trigger Devices 264
- 5-21 One-Shot (Monostable Multivibrator) 264
- 5-22 Clock Generator Circuits 268
- 5-23 Troubleshooting Flip-Flop Circuits 271
- 5-24 Sequential Circuits in PLDs Using Schematic Entry 276
- 5-25 Sequential Circuits Using HDL 280
- 5-26 Edge-Triggered Devices 284
- 5-27 HDL Circuits with Multiple Components 289

CHAPTER 6 Digital Arithmetic: Operations and Circuits 308

- 6-1 Binary Addition and Subtraction 310
- 6-2 Representing Signed Numbers 311
- 6-3 Addition in the 2's-Complement System 318
- 6-4 Subtraction in the 2's-Complement System 319
- 6-5 Multiplication of Binary Numbers 322
- 6-6 Binary Division 323
- 6-7 BCD Addition 324
- 6-8 Hexadecimal Arithmetic 326
- 6-9 Arithmetic Circuits 329
- 6-10 Parallel Binary Adder 330
- 6-11 Design of a Full Adder 332

- 6-12 Complete Parallel Adder with Registers 335
- 6-13 Carry Propagation 337
- 6-14 Integrated-Circuit Parallel Adder 338
- 6-15 2's-Complement Circuits 340
- 6-16 ALU Integrated Circuits 343
- 6-17 Troubleshooting Case Study 347
- 6-18 Using Altera Library Functions 349
- 6-19 Logical Operations on Bit Arrays with HDLs 356
- 6-20 HDL Adders 357
- 6-21 Parameterizing the Bit Capacity of a Circuit 359

CHAPTER 7 Counters and Registers 374

- 7-1 Asynchronous (Ripple) Counters 376
- 7-2 Propagation Delay in Ripple Counters 380
- 7-3 Synchronous (Parallel) Counters 382
- 7-4 Counters with MOD Numbers $<2^N$ 385
- 7-5 Synchronous Down and Up/Down Counters 392
- 7-6 Presettable Counters 394
- 7-7 IC Synchronous Counters 396
- 7-8 Decoding a Counter 406
- 7-9 Analyzing Synchronous Counters 409
- 7-10 Synchronous Counter Design 413
- 7-11 Altera Library Functions for Counters 421
- 7-12 HDL Counters 426
- 7-13 Wiring HDL Modules Together 438
- 7-14 State Machines 446
- 7-15 Register Data Transfer 458
- 7-16 IC Registers 458
- 7-17 Shift Register Counters 467
- 7-18 Troubleshooting 471
- 7-19 Megafunction Registers 474
- 7-20 HDL Registers 477
- 7-21 HDL Ring Counters 484
- 7-22 HDL One-Shots 485

CHAPTER 8 Integrated-Circuit Logic Families 514

- 8-1 Digital IC Terminology 516
- 8-2 The TTL Logic Family 525
- 8-3 TTL Data Sheets 529
- 8-4 TTL Series Characteristics 533
- 8-5 TTL Loading and Fan-Out 536
- 8-6 Other TTL Characteristics 541

- 8-7 MOS Technology 545
- 8-8 Complementary MOS Logic 548
- 8-9 CMOS Series Characteristics 550
- 8-10 Low-Voltage Technology 557
- 8-11 Open-Collector/Open-Drain Outputs 560
- 8-12 Tristate (Three-State) Logic Outputs 565
- 8-13 High-Speed Bus Interface Logic 568
- 8-14 The ECL Digital IC Family 570
- 8-15 CMOS Transmission Gate (Bilateral Switch) 573
- 8-16 IC Interfacing 575
- 8-17 Mixed-Voltage Interfacing 580
- 8-18 Analog Voltage Comparators 581
- 8-19 Troubleshooting 583
- 8-20 Characteristics of an FPGA 585

CHAPTER 9 MSI Logic Circuits 604

- 9-1 Decoders 605
- 9-2 BCD-to-7-Segment Decoder/Drivers 613
- 9-3 Liquid-Crystal Displays 615
- 9-4 Encoders 619
- 9-5 Troubleshooting 625
- 9-6 Multiplexers (Data Selectors) 627
- 9-7 Multiplexer Applications 633
- 9-8 Demultiplexers (Data Distributors) 638
- 9-9 More Troubleshooting 645
- 9-10 Magnitude Comparator 649
- 9-11 Code Converters 652
- 9-12 Data Busing 656
- 9-13 The 74ALS173/HC173 Tristate Register 657
- 9-14 Data Bus Operation 660
- 9-15 Decoders Using HDL 666
- 9-16 The HDL 7-Segment Decoder/Driver 670
- 9-17 Encoders Using HDL 673
- 9-18 HDL Multiplexers and Demultiplexers 676
- 9-19 HDL Magnitude Comparators 680
- 9-20 HDL Code Converters 681

CHAPTER 10 Digital System Projects Using HDL 704

- 10-1 Small-Project Management 706
- 10-2 Stepper Motor Driver Project 707
- 10-3 Keypad Encoder Project 715
- 10-4 Digital Clock Project 721

- 10-5 Microwave Oven Project 738
- 10-6 Frequency Counter Project 745

CHAPTER 11 Interfacing with the Analog World 754

- 11-1 Review of Digital Versus Analog 755
- 11-2 Digital-to-Analog Conversion 757
- 11-3 DAC Circuitry 764
- 11-4 DAC Specifications 769
- 11-5 An Integrated-Circuit DAC 771
- 11-6 DAC Applications 772
- 11-7 Troubleshooting DACs 774
- 11-8 Analog-to-Digital Conversion 775
- 11-9 Digital-Ramp ADC 776
- 11-10 Data Acquisition 781
- 11-11 Successive-Approximation ADC 785
- 11-12 Flash ADCs 792
- 11-13 Other A/D Conversion Methods 794
- 11-14 Typical ADC Architectures for Applications 800
- 11-15 Sample-and-Hold Circuits 800
- 11-16 Multiplexing 801
- 11-17 Digital Signal Processing (DSP) 802
- 11-18 Applications of Analog Interfacing 806

CHAPTER 12 Memory Devices 824

- 12-1 Memory Terminology 827
- 12-2 General Memory Operation 830
- 12-3 CPU-Memory Connections 833
- 12-4 Read-Only Memories 835
- 12-5 ROM Architecture 837
- 12-6 ROM Timing 839
- 12-7 Types of ROMs 840
- 12-8 Flash Memory 848
- 12-9 ROM Applications 852
- 12-10 Semiconductor RAM 855
- 12-11 RAM Architecture 855
- 12-12 Static RAM (SRAM) 857
- 12-13 Dynamic RAM (DRAM) 862
- 12-14 Dynamic RAM Structure and Operation 863
- 12-15 DRAM Read/Write Cycles 868
- 12-16 DRAM Refreshing 869
- 12-17 DRAM Technology 871
- 12-18 Other Memory Technologies 873

- 12-19 Expanding Word Size and Capacity 876
- 12-20 Special Memory Functions 884
- 12-21 Troubleshooting RAM Systems 886
- 12-22 Testing ROM 892

CHAPTER 13 Programmable Logic Device Architectures 908

- 13-1 Digital Systems Family Tree 910
- 13-2 Fundamentals of PLD Circuitry 915
- 13-3 PLD Architectures 917
- 13-4 The Altera MAX7000S Family 922
- 13-5 The Altera MAX II Family 926
- 13-6 The Altera Cyclone Series 930

Glossary 936

Answers to Selected Problems 949

Index of ICs 957

Index 961