

CONTENTS

Preface	v	
EXPERIMENT 1	Preliminary Concepts	1
EXPERIMENT 2	Logic Gates I: OR, AND, and NOT	7
EXPERIMENT 3	Troubleshooting OR, AND, and NOT Gates	13
EXPERIMENT 4	Basic Combinatorial Circuits	27
EXPERIMENT 5	Logic Gates II: NOR and NAND	33
EXPERIMENT 6	Troubleshooting NOR and NAND Gates	39
EXPERIMENT 7	Boolean Theorems	47
EXPERIMENT 8	Simplification Using Boolean Theorems	51
EXPERIMENT 9	DeMorgan's Theorems	55
EXPERIMENT 10	The Universality of NAND and NOR Gates	61
EXPERIMENT 11	Implementing Logic Circuit Designs	67
EXPERIMENT 12	Exclusive-OR and Exclusive-NOR Circuits	71
EXPERIMENT 13	Designing with Exclusive-OR and Exclusive-NOR Circuits	77
EXPERIMENT 14	Troubleshooting Exclusive-OR and Combinatorial Circuits	81
EXPERIMENT 15	Flip-Flops I: Set/Clear Latches and Clocked Flip-Flops	85
EXPERIMENT 16	Flip-Flops II: D Latch; Master/Slave Flip-Flops	93
EXPERIMENT 17	Schmitt Triggers, One-Shots, and Astable Multivibrators	99
EXPERIMENT 18	Designing with Flop-Flop Devices	107
EXPERIMENT 19	Troubleshooting Flip-Flop Circuits	115
EXPERIMENT 20	Binary Adders and 2's Complement System	123
EXPERIMENT 21	Asynchronous IC Counters	131
EXPERIMENT 22	A BCD Counter	137
EXPERIMENT 23	Synchronous IC Counters	143
EXPERIMENT 24	IC Counter Application: Frequency Counter	151

EXPERIMENT 25	Troubleshooting Counters: Control Waveform Generation 157
EXPERIMENT 26	Shift Register Counters 163
EXPERIMENT 27	IC Registers 167
EXPERIMENT 28	Designing with Counters and Registers 173
EXPERIMENT 29	TTL and CMOS IC Families – Part I 177
EXPERIMENT 30	TTL and CMOS IC Families – Part II 187
EXPERIMENT 31	Using a Logic Analyzer 195
EXPERIMENT 32	IC Decoders 207
EXPERIMENT 33	IC Encoders 215
EXPERIMENT 34	IC Multiplexers and Demultiplexers 221
EXPERIMENT 35	Troubleshooting Systems Containing MSI Logic Circuits 231
EXPERIMENT 36	IC Magnitude Comparators 235
EXPERIMENT 37	Data Busing 239
EXPERIMENT 38	Digital-to-Analog Converters 249
EXPERIMENT 39	Analog-to-Digital Converters 255
EXPERIMENT 40	Semiconductor Random Access Memory (RAM) 261
EXPERIMENT 41	Synchronous Counter Design 271
EXPERIMENT 42	Programmable Function Sequencer 277

SUPPLEMENTAL EXPERIMENTS 283

EXPERIMENT S1	Logic Gates: OR, AND, and NOT 285
EXPERIMENT S2	Basic Combinatorial Circuits 291
EXPERIMENT S3	Logic Gates: NOR and NAND 303
EXPERIMENT S4	Boolean Theorems 311
EXPERIMENT S5	Simplification Using Boolean Theorems 323
EXPERIMENT S6	DeMorgan's Theorems 333
EXPERIMENT S7	Implementing Logic Gates and Circuits Using VHDL 343
EXPERIMENT S8	Implementing Logic Circuit Designs 351
EXPERIMENT S9	Exclusive-OR and Exclusive-NOR Circuits 361
EXPERIMENT S10	Designing with Exclusive-OR and Exclusive-NOR Circuits 369
EXPERIMENT S11	Implementing Exclusive-OR and Exclusive-NOR Circuits Using VHDL 387
EXPERIMENT S12	Latches and D-Type Flip-Flops 395
EXPERIMENT S13	J-K and T-Type Flip-Flops 415
EXPERIMENT S14	Flip-Flop Applications 429
EXPERIMENT S15	Implementing Flip-Flops and Flip-Flop Devices with VHDL 447
EXPERIMENT S16	Binary Adders and 2's Complement System 457
EXPERIMENT S17	Asynchronous Counters 471
EXPERIMENT S18	Synchronous Counters 483
EXPERIMENT S19	BCD Counters 497
EXPERIMENT S20	Shift Register Counters 507
EXPERIMENT S21	IC Registers 517
EXPERIMENT S22	One-Shots, Counters, and Registers with VHDL 531
EXPERIMENT S23	IC Decoders and Encoders 545
EXPERIMENT S24	IC Multiplexers and Demultiplexers 555
EXPERIMENT S25	VHDL State Machines 565
PROJECT SP1	Implementing a Simple Frequency Counter 579
Appendix A	Wiring and Troubleshooting Digital Circuits 589
Appendix B	Logic Analyzers 597
Appendix C	Manufacturers' Data Sheets 613
Appendix D	Using Quartus® II and Programming PLD Boards with Quartus® II Projects 641